# A SIMPLE MODEL FOR STRESS VOIDING IN PASSIVATED THIN FILM CONDUCTORS

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## ABSTRACT

A model is proposed for stress voiding in passivated thin film conductors. The rate limiting step is argued to be the formation of vacancies at dislocation jogs which then diffuse to void sites.

## INTRODUCTION

Considerable effort has been expended to understand an insidious failure mode in passivated thin metal film conductors called "stress voiding". [1-7] It has been pretty well accepted that the failure mechanism is a form of diffusive creep relieving stress caused by the difference in the coefficients of thermal expansion between the metal conductor and the surrounding media and the temperature excursions experienced during integrated circuit processing. It has been demonstrated, both theoretically and experimentally that these thermally induced stresses are quite large, nearly hydrostatic and independent of the retained stress in the overlying passivation material. They are dependent primarily on the temperature history and to a lesser degree on the geometry. [8]

In this paper, a simple model of the process of stress voiding is proposed where void formation and growth are the products of a stress induced vacancy supersaturation generated by dislocation climb, and the subsequent diffusion of these vacancies to voids. The following model also has the feature of being consistent with hydrostatic stress relief.

## MODEL

Consider a metal line deposited at an elevated temperature onto a Silicon substrate (or one which had been held at high temperature for a sufficiently long time so as to permit stress relief). While at high temperature, a strong passivation material possessing a much smaller thermal coefficient of expansion (TCE) than the metal, in this case, identical to the substrate, is applied. The sample is then cooled relatively rapidly. Since the enclosed metal film has a larger coefficient of expansion than the passivation, it will "want" to assume a smaller volume than that enclosed by the passivation. If the adhesion is good and the passivation is so thick as to not be appreciably distorted, the amount of stress, $\sigma$, retained in the metal conductor is;

$$\sigma = \beta \Delta\alpha \Delta T \qquad (1)$$

where $\Delta\alpha$ is the difference in the TCE'S of the metal and the substrate/passivation system and $\Delta T$ is the difference in temperature between the application of the passivation and the temperature of observation. $\beta$ is the bulk modulus. In this idealized picture, the stress will be in hydrostatic tension. Under more realistic conditions, the picture would become somewhat more complicated, but the complexity will not contribute to understanding the general mechanism of void formation and growth.

Note for a temperature difference of a few hundred degres, typical of IC processing, the expected stress is extremely high. Stresses close to 0.5% of the Bulk Modulus can be expected,

or about five times the tensile yield stress. [8] The nearly hydrostatic nature of the stress keeps the stress from being relieved by dislocation glide.

Although dislocation glide cannot relieve hydrostatic stresses, dislocation climb can until the vacancy concentration in thermal equilibrium with the stress is attained Dislocation climb is accompanied by the formation or the annihilation of vacancies depending on the sign of the motion. A dislocation climbing under the influes the vibrational frequency of the lattice ($10^{13}$/sec) and $\Delta H^f_v$ is the activation free energy of vacancy formation. The vacancy formation will continue until;

$$C_\sigma = C_v \exp(-\sigma\Omega / kT) \qquad (2)$$

where $C_v$ is the thermal equilibrium vacancy concentration in the absence of stress and $\Omega_v$ is the vacancy volume. For Al, this can be shown to be a very efficient process even at low temperatures. Each dislocation leaves behind the equivalent of a sheet of vacancies which disperse throughout the crystal. It can be shown that only a single dislocation need climb through a 1 um cube crystal to produce a vacancy concentration in equilibrium with the thermal stress.

It is interesting to note that despite their near ubiquity, it can be shown that the nucleation of voids is theoretically impossible without the unsatisfying necessity of "deus ex machina" stress concentrations. [9] These stress concentrations, which undoubtedly exist, determine the location of void nucleation, characteristically at film edges or sites of known high stress such as at steps in the underlying substrate. It has also been suggested, however, that delaminations between the surface metal and the passivation are sufficient to nucleate voids without the classical nucleation problem. [7] The shape of the voids is probably determined by random fluctuations in grain orientation rather than surface energy considerations. [10]

Once formed, voids grow by the diffusion of vacancies provided by dislocation climb to the stress free void surface. Consider a thin narrow conductor with a "bamboo" structure containing voids at some of the grain boundaries with an average spacing of $2l_v$. (Fig.1) Vacancy diffusion along grain boundaries to the voids is assumed to be very rapid (in fact, instantaneous) compared to lattice diffusion. The flux of vacancies into a void will, therefore, be equal to the flux of lattice vacancies into a grain boundary with a void. This approximation simplifies the geometry for the calculation significantly, leaving us with a simple 1 dimensional boundary value problem. The case of a polycrystalline film will require the use of a more complicated geometry, which will be the subject of future work, but will not differ in concept from what is treated here.

As vacancies diffuse to the grain boundaries, they are replaced via dislocation climb at a rate given by

$$K = \frac{N_d}{a^2 v_d}$$

where Arrhenius is the dislocation density expressed in length of dislocation per unit volume, a is the lattice constant and $v_d$ is the drift velocity of the climbing dislocation given by

$$v_d = \frac{D_d F}{kT} \qquad (3)$$

where $D_d$ is the dislocation diffusivity and F is the driving force on the dislocation given by;

$$Fb = kT \ln\left(\frac{C_\sigma}{C}\right) = \sigma\Omega_v - kT \ln\left(\frac{C_o}{C}\right) \qquad (3a)$$

where b is the burgers vector of the dislocation. F will be the chemical potential gradient from the dislocation jog generating site to the surrounding medium. If vacancy formation at jogs is the rate limiting step, the activation energy for dislocation climb will be the same as that for vacancy formation. Since vacancy diffusion is a faster process than vacancy formation, the second term in eqn. (3a) can be neglected and a steady state concentration profile will be achieved expressed by the solution to;

$$D_v\left(\frac{\partial^2 C}{\partial x^2}\right) + K = 0 \tag{4}$$

where $D_v$ is the vacancy diffusivity according to the boundary condition that the vacancy concentration is at the thermal equilibrium value, $C_0$, at the grain boundaries ($x = \pm l_v$). Grain boundaries not containing voids can be ignored since they will be in thermal equilibrium with the lattice. Grain boundary grooving is not considered. The solution to (4) according to the stated boundary conditions is simply;

$$C - C_o = N_d\left(\frac{D_d}{D_v}\right)\frac{\sigma}{2kT}\left(l_v^2 - x^2\right) \tag{5}$$

recognizing that $a^2 b \sim \Omega$.

The vacancy flux contributing to void growth will be twice the flux calculated from the spatial derivative of eqn. (5), since each grain boundary is fed by both of the adjacent diffusion fields on either side. Void growth rate will be;

$$\frac{\partial V(t)}{\partial t} = 2D_d\Omega_v w\tau\frac{\partial C(l_v)}{\partial x} = \frac{2D_d\sigma N_d\Omega_v(l_v w\tau)}{kT} \tag{6}$$

where w is the film width, and $\tau$ is the film thickness.

Since the reliability of an integrated circuit can be determined by a stress void which grows to a size on the order of the line width, stress induced void growth kinetics are an important engineering topic. Curiously, reliability engineers appear to have a passionate love affair with the Arrhenius relation, to the exclusion of entertaining all others. Unfortunately, as any metallurgy student can tell you, M. Nature does not always favor such simple kinetics. Stress voiding is one such process which does not cooperate. In order to relate to previous work, we will define kinetics in terms of the derivative of the logarithm of the void growth rate with the Metallizations temperature as one would for a purely thermally activated process.

During void growth, thermal stresses are continuously being relieved by the dislocation climb/vacancy diffusion process outlined above. Since stress appears as the driving force for dislocation climb, and therefore void growth in eqn. (3) stress relief must be considered when discussing void growth kinetics. Realizing that the stress will be reduced by vacancy diffusion to the void we need to rewrite eqn. (6) to incorporate this;

$$\frac{\partial V(t)}{\partial t} = \left(\frac{2D_d\Omega_v\beta}{kT}\right)\left[\Delta\alpha(T_o - T) - \left(\frac{1}{l_v w\tau}\right)\int_0^t \frac{dV(t)}{dt}dt\right] \tag{7}$$

Realizing that the integral in eqn. (7) is simply the void volume, V(t);

$$\frac{dV(t)}{dt} + \Phi V(t) - \Phi\Psi = 0 \tag{8}$$

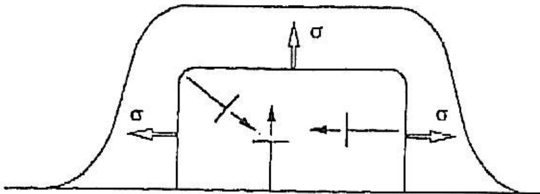


Figure 1. Schematic of cross section of typical passivated integrated circuit conductor. The differential thermal expansion provides for a nearly hydrostatic stress. Dislocations, possibly generated as a response to non-hydrostatic components of the thermal stress, interior to the grain are sources of vacancies contributing to void growth.

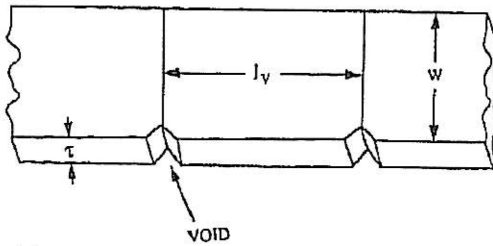


figure 2. Schematic of the geometry represented in the model. Voids are assumed to be nucleated at grain boundariesseperated by a distance, $l_v$, in a bamboo structure thin film w wide and τ thick.

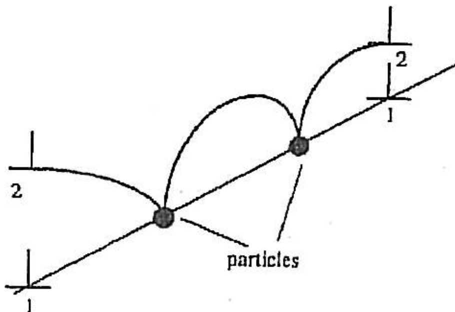


Figure 3. Schematic of possible mechanism to inhibit voids. small particles can inhibit the climb of dislocations and thereby slow the generation of vacancies required for void growth.

where

$$\Psi = l_v w \tau \Delta\alpha \Delta T$$

and

$$\Phi = \frac{2D_d \Omega_v \beta}{kT}$$

The void volume as a function of time is;

$$V(t) = V_{\infty}\left[1 - \exp(-\Phi t)\right] \quad (9)$$

where it is recognized that $\Psi$ is the ultimate void volume after infinite time, $V_{\infty}$. The change in $D_d$ with reduced stress has been ignored for computational simplicity and should not appreciably affect the solution. If it is assumed, incorrectly, that the void growth rate is purely thermally activated, an apparent activation energy can be obtained from the differentiation of the logarithm of the void growth rate with the reciprocal of the temperature.

$$\Delta H_{app} = \Delta H_f(1 - t\Phi) - \frac{kT^2}{(T_o - T)} \quad (10)$$

which hardly looks like an Arrhenius relation. It is dependent on the temperature of the observation, the temperature at which the passivation was applied and with time.

For finer grain sizes, the 1 dimensional problem above must be replaced by a solution to an appropriate 2 dimensional geometry, but will, in principle, be similar.

## DISCUSSION

The preceding model correctly predicts the distinctly non-Arrhenius behavior observed in stress voiding. This is not unique to this model, of course. A distinct feature, however, is that it offers a mechanism for relaxation of the principally hydrostatic stresses observed in passivated thin films. The behavior predicted in this model suggests the possibility of producing a series of TTT type diagrams for films of various alloys passivated at different temperatures. TTT diagrams may be useful in deciding whether and to what extent a problem will exist given various thermal histories.

The major difference between this model and the others is that in this model, we are concerned with the generation and migration of vacancies to relieve the stresses induced by thermal expansion. The major determining parameter for void growth will be in the intervoid distance. Grain size, although of some consequence will be less important.

An important component of this model is role of dislocations in the void growth process. It is interesting that a recent UHVTEM study has observed a high dislocation density in grains with well developed voids. [11] One important feature of this model is that the perceived panacea of producing "bamboo" structure films will not work. Grain boundaries are not needed to transport metal atoms away from the void. This process could, in principle, be operating in a single crystal, providing voids could be nucleated. In fact, a scenario could be created where a bamboo film with fewer voids on grain boundaries of nearly parallel orientation would be a much greater reliability risk than a fine grain film with more voids. It is conceivable that void growth, with equal stress, could be faster in a bamboo film than in one with many grain boundary paths. A recent study suggests such an effect. [12]

The model also suggests methods for reducing the propensity for voiding. Dislocation climb is a structure sensitive process, in that it can be impeded by obstacles. Metallizations containing

finely disbursed particles or precipitates should be less vulnerable to stress voiding. Sigma in eqn. (3) could be replaced by $\sigma - \sigma_p$, where $\sigma_p$ is a threshold stress required to free the climbing dislocation from the particle given by $\sigma_p = K_p (G\, b/l_p)$ where $K_p$ is a constant, G is the shear modulus and $l_p$ is the particle spacing. Opportunities for new alloy development considering this may be there, providing high conductivity is maintained.

The design of accelerated tests is an important part of any reliability engineer's job. These tests must be capable of providing information for conditions typical of use, yet must be obtained in a short time. It is, therefore, very important to fully understand the mechanism being investigated. With the plethora of stress void models proposed over the past few years, this is an uncomfortable task. Clever experimentalists must attack this problem and perform the "critical test" of the theories. Only then can we feel comfortable using any model for predicting reliability in integrated circuits.

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